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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,768	01/27/2004	Ronald Duane McCallister	2298-010	3629

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2611	

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03/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,768	MCCALLISTER, RONALD DUANE	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 1/16/09, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 11-13, 15-16, 18, 20, 22, 24 29, are rejected under 35 U.S.C. 103(a) as being unpatentable over by Chandrasekaran U.S. Pub No 2003/0174783 A1 in view of Jeckeln et al U.S. Pub no 20020191710 A1.

As per claim 1 Chandrasekaran teaches a predistortion circuit for compensating linear distortion introduced by analog-transmitter components of a digital communications transmitter, said predistortion circuit comprising: a source of a complex-forward-data stream configured to digitally convey information (see fig.3 elements 304-306 and page 2 [0020]) within a bandwidth; a digital equalizer section coupled to said complex- forward-data-stream source and configured to generate an equalized-complex-forward-data stream and to pass said equalized-complex-forward-data stream to said analog- transmitter components ((see fig.3 element 308 and page 2 [0020]); a feedback section adapted to receive a feedback signal from said analog-transmitter components and configured to provide a complex-return-data stream (see abstract and fig.3 elements 330, 332, 334 and page 2 [0020]) ; and a controller (see fig.3 element 336, 316, 318 and page 2 [0020] and page 2 [0021]) coupled to said feedback section and to said equalizer section and configured so that said equalizer section compensates for frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components (see page 3 [0023] [0031-0034] and page 4 and page [0060]).

However Chandrasekaran does not teach a feedback section comprising a complex-digital-subharmonic sampling down converter adapted to receive a feedback

signal from said analog-transmitter components, and configured to provide a complex-return-data stream at greater than or equal to said bandwidth.

Jeckeln teaches a feedback section comprising a complex digital sampling down converter is functionally equivalent to the claimed (complex-digital-subharmonic sampling down converter) (see figs. 1-2, 4a-4b elements 52 and 54 or 58 and 60 combined and page 3 paragraph [0067] and page 4 [0069]) adapted to receive a feedback signal from said analog-transmitter components, and configured to provide a complex-return-data stream at greater than or equal to said bandwidth.

It would have bee obvious to one of ordinary skill in the art to implement the teaching of Jeckeln into Chandrasekaran as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claims 2, Chandrasekaran et al inherently teaches a predistortion circuit as claimed in claim 1 wherein said analog-transmitter components include a power amplifier having an input and an output (see fig.3 element 314 or 326) and said feedback section comprises: a first analog input (see fig.3 element 330) adapted to receive a first RF-analog signal from said power amplifier input; and a second analog input (see fig.3 element 330) adapted to receive a second RF- analog signal from said power amplifier output. Furthermore implementing such teaching into Jeckeln would have been obvious to one skilled in the art as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claims 11, Chandrasekaran inherently teaches predistortion circuit as claimed in claim 1 wherein said equalizer section implements a complex equalizer (see fig.3 element 308 and [0031]).

As per claim 12, Chandrasekaran inherently teaches predistortion circuit as claimed in claim 1 wherein: said complex-forward-data stream exhibits a forward resolution (abstract); and said complex-return-data stream exhibits a return resolution less than said forward resolution (see fig.3). Furthermore implementing such teaching into Jeckeln would have been obvious to one skilled in the art as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claim 13, Chandrasekaran inherently teaches wherein said feedback section generates said complex-return- data stream so that said return resolution is at most four bits less than said forward resolution. Furthermore implementing such teaching into Jeckeln would have been obvious to one skilled in the art as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claim 15, Chandrasekaran inherently teaches, predistortion circuit as claimed in claim 1 additionally comprising a delay module is the same as the claimed (programmable delay element) coupled between said complex-forward-data-stream source and said feedback section, said programmable delay element being configured

to produce a delayed-complex-forward-data stream temporally aligned with said complex-return-data stream (see page 1 [0013-0017]). Furthermore implementing such teaching into Jeckeln would have been obvious to one skilled in the art as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claim 16, Chandrasekaran and Jeeckln in combination would teach said complex-forward-data stream propagates through said predistortion circuit in response to a clock signal and said a delay module is the same as the claimed (programmable delay element) includes an integral section that delays at least a portion of said complex-forward- data stream by an integral number of cycles of said clock signal and includes a fractional section that delays said portion of said complex-forward-data stream by a fraction of a cycle of said clock signal as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claim 18, Chandrasekaran inherently teaches wherein said controller is configured to cause said a delay module is the same as the claimed (programmable delay element) to temporally align said delayed- complex-forward-data stream with said complex-return-data stream prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components (see page 1 [0013-0017]). Furthermore implementing such teaching into Jeckeln would have been obvious to one skilled in the art as to

ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claims 20, Chandrasekaran and Jeeckln in combination would teach wherein: said analog-transmitter components include a band-pass filter which inserts a band-pass-filter delay; and said predistortion circuit additionally comprises a phase rotator configured to rotate one of said complex-forward-data and complex-return-data streams relative to the other to compensate for said band-pass-filter delay as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claim 22, Chandrasekaran and Jeeckln in combination would teach wherein said controller is configured to cause said phase rotator to compensate for said band-pass-filter delay prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claim 24, Chandrasekaran inherently teaches a predistortion circuit as claimed in claim 1 wherein said equalizer section includes a first equalizer (see fig.3 element 308) configured to filter said complex-forward-data stream and a second equalizer (see fig.3 element 320) configured to filter said complex-return-data stream. Furthermore implementing such teaching into Jeckeln would have been obvious to one

skilled in the art as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

As per claims 29, Chandrasekaran inherently teaches wherein: said analog section includes a power amplifier(see fig.3 element 314), which exhibits a gain; and said predistortion circuit additionally comprises an adjustable attenuation circuit configured to compensate for said gain of said power amplifier and positioned to process said complex-return-data stream before filtering in said second equalizer (see fig.3 element 320). Furthermore implementing such teaching into Jeckeln would have been obvious to one skilled in the art as to ensure that the IQ modulator correctly distort the RF signal so that the digital receiver could accurately compensate for delay introduced by the Power amplifier as taught by Jeckeln (see Page 4 [0069]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-10, 17, 19, 21, 23, 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chandrasekaran U.S. Pub No 2003/0174783 A1 view of Jeckeln et al U.S. Pub no 20020191710 A1 and in further view of Sarca U.S. Pub No 2005/0123066 A1.

5. As per claim 3, Chandrasekaran and Jeckeln in combination teach all the features of the claimed invention except wherein said controller is configured to compensate for linear distortion in an RF-analog signal present at said input of said power amplifier, and then compensate for linear distortion in an amplified RF signal present at said output of said power amplifier.

6. Sarca teaches predistortion circuit controller configured to compensate for linear distortion in an RF-analog signal present at said input of said power amplifier, then compensate for linear distortion in an amplified RF signal present at said output of said power amplifier (see figs.4-5 element 7 and page 4 [0061] and page 5 [0069]).

7. It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Chandrasekaran and Jeckeln combination as to provide a correction for linear distortions outside the up-conversion chain and determine adjustment needed in accordance with adaptation algorithm as taught by Sarca (see page 5 [0069]).

As per claim 4 , Chandrasekaran and Jeckeln in combination teach all the features of the claimed invention except wherein said equalizer section comprises: a non-adaptive equalizer configured to be programmed with filter coefficients; and an adaptation engine coupled to said non-adaptive equalizer and configured to implement an estimation-and- convergence algorithm which determines said filter coefficients.

Sarca teaches a non-adaptive equalizer configured to be programmed with filter coefficient (see fig.4 page 5 [0063]; and an adaptation engine (see fig.4 element 74

coupled to said non-adaptive equalizer and configured to implement an estimation-and-convergence algorithm which determines said filter coefficients (see page 4 [0051]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Chandrasekaran and Jeckeln combination so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 5, Chandrasekaran, Jeckeln and Sarca in combination would teach wherein said non-adaptive equalizer processes said complex-forward-data stream, and said adaptation engine is responsive to said complex-forward-data stream and said complex-return-data stream so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 6 and 25, Chandrasekaran, Jeckeln and Sarca in combination in combination would teach: said non-adaptive equalizer is a complex equalizer having an in-phase path, a quadrature path, an in-phase-to-quadrature path, and a quadrature-to-in-phase path; a first set of said filter coefficients is programmed in said in-phase and quadrature paths, and a second set of said filter coefficients is programmed in said in-phase-to- quadrature and quadrature-to-in-phase paths; and said adaptation engine accommodates a partial complex equalizer and has first and second paths, said first and second paths being configured in one mode to determine said filter coefficients for said in-phase and quadrature paths, and being configured in another mode to determine said filter coefficients for said in-phase-to-quadrature and quadrature-to- in-phase paths

so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 7 , Chandrasekaran, Jeckeln and Sarca in combination would teach wherein said equalizer section implements an estimation-and-convergence algorithm to determine filter coefficients (see Sarca page 4 [0051] and page 5 [0063]) that compensate for said frequency dependent quadrature gain and phase imbalance so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 8, 10, Chandrasekaran, Jeckeln and Sarca in combination would teach: said estimation-and-convergence algorithm is responsive to said complex-forward-data stream and to said complex-return- data stream; said complex-forward-data stream and said complex-return- data stream exhibit forward-error and return-error levels, respectively, with said return-error level being greater than said forward-error level (see page 5 [0064]); and said estimation-and-convergence algorithm is configured to transform increased algorithmic processing time into reduced effective-error level for said complex-return-data stream so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 9, Chandrasekaran, Jeckeln and Sarca in combination would teach wherein said estimation-and-convergence algorithm causes said equalizer section to converge at said filter coefficients after processing a multiplicity of samples from said complex-return- data stream so that the adaptive algorithm would become the optimal

one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 17 , Chandrasekaran and Jeckeln in combination teach all the features of the claimed invention except: said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said feedback section and having an output coupled to said controller; and said controller and said correlator are configured to implement an estimation-and-convergence algorithm to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream.

Sarca teaches said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said feedback section and having an output coupled to said controller; and said controller and said correlator (see page 3 [0047-0048]) are configured to implement an estimation-and-convergence algorithm to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream (see page 5 [0067] and page 6 [0074-0075]).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Chandrasekaran and Jeckeln combination as to track the changes in the power amplifier characteristics and preserve the maximum achievable performance in time and with environment variations as taught by Sarca (see page 6 [0077]).

As per claims 19 and 23, Chandrasekaran, Jeckeln and Sarca in combination would teach wherein: said equalizer section comprises an adaptive equalizer configured to determine filter coefficients (see Sarca page 5 [0063]) that compensate for said frequency dependent quadrature gain and phase imbalance; and said adaptive equalizer increases correlation (see Sarca page 3 [0048]) between said delayed-complex-forward-data stream and said complex-return- data stream in determining said filter coefficients so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claim 21, Chandrasekaran, Jeckeln and Sarca in combination would teach wherein said phase rotator is configured to implement an estimation-and-convergence algorithm (see Sarca page 4 [0051] to determine an amount of phase rotation that compensates for said band-pass-filter delay so that the adaptive algorithm would become the optimal one and produce a solution in exactly one iteration as taught by Sarca (see page 4, [0051]).

As per claims 26, 27 Chandrasekaran and Jeckeln in combination teach all the features of the claimed invention except wherein said controller is configured to cause said feedback section to monitor said first RF-analog signal while adjusting said first equalizer to compensate for linear distortion at said input of said power amplifier, then cause said feedback section to monitor said second RF-analog signal while further adjusting said first equalizer to compensate for linear distortion at said output of said power amplifier.

8. Sarca teaches wherein said controller is configured to cause said feedback section to monitor said first RF-analog signal while adjusting said first equalizer to compensate for linear distortion at said input of said power amplifier, then cause said feedback section to monitor said second RF-analog signal while further adjusting said first equalizer to compensate for linear distortion at said output of said power amplifier (see figs.4-5 element 7 and page 4 [0061] and page 5 [0069]).

9. It would have been obvious to one of ordinary skill in the art to implement the teaching of Sarca into Chandrasekaran and Jeckeln combination as to provide a correction for linear distortions outside the up-conversion chain and determine adjustment needed in accordance with adaptation algorithm as taught by Sarca (see page 5 [0069]).

As per claim 28 Chandrasekaran, Jeckeln and Sarca in combination would teach said first equalizer is adjusted to increase correlation between said second RF-analog signal and a first signal -84- responsive to said complex-forward-data stream and having a first bandwidth; and said second equalizer is adjusted to increase correlation between said second RF-analog signal and a second signal responsive to said complex-forward-data stream and having a second bandwidth wider than said first bandwidth as to provide a correction for linear distortions outside the up-conversion chain and determine adjustment needed in accordance with adaptation algorithm as taught by Sarca (see page 5 [0069]).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Rosenlog et al U.S. Pub NO 20040224715 A1.

12. Nadiri U.S. Pub No 20040165678 A1.

13. Ding et al U.S. Pub NO 20050069050 A1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571 272 3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

3/26/2009

Emmanuel Bayard
Primary Examiner
Art Unit 2611

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